PATENT ABSTRACTS OF JAPAN

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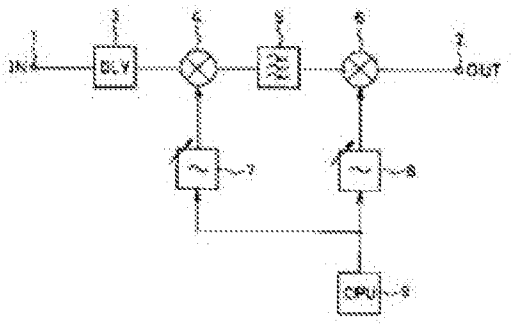
(54) FREQUENCY CONVERTING DEVICE

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a frequency converting device, which easily meets a desired characteristic by absorbing variations in changes of local frequency without changing a characteristic of a group delay equalizer to the fluctuation of a group delay amount and also is inexpensive and small.
SOLUTION: A frequency-converting device that includes an equalizer, which equalizes group delay distortion that occurs in a band pass filter which is mounted on an intermediate frequency of a double conversion system is provided with a 1st mixer 4 which undergoes frequency conversion of an input signal, a 1st synthesizer 7 which is connected to a local terminal of the mixer 4, a band-pass filter 5 which is connected to an output terminal of the mixer 4, a 2nd mixer 6 which is connected to an output terminal of the filter 5 and a 2nd synthesizer 8, which is connected to a local terminal of the mixer 6 and makes an output terminal of the mixer 6 its output.



* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1]In a power converter having an equalizer for equalizing group-delay distortion generated with a band pass filter mounted in an intermediate frequency of a double conversion system, The 1st mixer that carries out frequency conversion of the input signal, and the 1st synthesizer connected to a terminal from an office of said 1st mixer, A band pass filter connected to an output terminal of said 1st mixer, and the 2nd mixer connected to an output terminal of said band pass filter, A power converter characterized by what it has the 2nd synthesizer connected to a terminal from an office of said 2nd mixer, and an output terminal of said 2nd mixer is considered for as an output.
[Claim 2]In a group-delay equalizer, the 1st mixer, a band pass filter, and a power converter provided with the 2nd mixer, A power converter characterized by a thing it was made to absorb dispersion in group-delay distortion for without making the characteristic of said group-delay equalizer variable by making it correspond to change of group delay quantity in said band pass filter, and changing frequency of a terminal from an office of said 1st and 2nd mixers.
[Claim 3]In a power converter having an equalizer for equalizing group-delay distortion generated with a band pass filter mounted in an intermediate frequency of a double conversion system, The 1st mixer that carries out frequency conversion of the input signal, and the 1st synthesizer connected to a terminal from an office of said 1st mixer, A band pass filter connected to an output terminal of said 1st mixer, and the 2nd mixer connected to an output terminal of said band pass filter, It has the 2nd synthesizer connected to a terminal from an office of said 2nd mixer, A power converter characterized by what consider an output terminal of said 2nd mixer as an output, an output frequency of said 1st and 2nd synthesizer is made to change according to a center gap of group-delay distortion of said band pass filter, and this absorbs dispersion in group-delay distortion for.
[Claim 4]The power converter according to claim 3, wherein said 1st and 2nd synthesizers comprised a digital PLL circuit and said 2nd synthesizer is made a frequency step is coarser than said 1st synthesizer, and possible [setting out].

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention]Especially this invention relates to the power converter formed in the transmission system or receiving system of a satellite communication device about a power

converter.
[0002]
[Description of the Prior Art]Conventionally, in this kind of power converter, in order that the group-delay equalizer for equalizing group-delay distortion may absorb manufacturing dispersion, the variable function is needed.
[0003]Although the composition of the large good transformation time delay equalizer of the variable range of the amount of group delay equalization is proposed by JP,H03-040534,B as a variable group-delay equalizer, without having an adverse effect on an amplitude frequency characteristic, After changing group delay quantity since the amplitude frequency characteristic of the group-delay equalizer itself is changed when changing group delay quantity, it is necessary to return degradation of an amplitude frequency characteristic.
[0004]Drawing 5 is a figure showing the composition of the conventional power converter. When drawing 5 is referred to, the conventional power converter, The 1st mixer 4 that carries out frequency conversion of the input signal, and the phase lock oscillator 11 connected to the terminal from an office of the 1st mixer 4, It has the band pass filter 5 connected to the output terminal of the 1st mixer 4, the 2nd mixer 6 connected to the output terminal of the band pass filter 5, and the synthesizer 8 connected to the terminal from an office of the 2nd mixer 6, and the output of the 2nd mixer 6 is connected to the output terminal 2, and it is constituted. 9 is logic for frequency setting, such as CPU, and 10 is a good transformation group-delay equalizer. Since a gap of group-delay distortion was equalized, in the conventional composition, it was absorbing with the good transformation group-delay equalizer 10.
[0005]
[Problem(s) to be Solved by the Invention]However, in order to realize a cheap and small power converter, it is necessary to absorb dispersion easily. Or what is necessary is just to make it not generate dispersion in group delay quantity.
[0006]In this case, when an intermediate frequency is low, can also solve the problem of dispersion in group delay quantity by using a digital filter so that it may be proposed by JP,S60-117926,A, for example, and the group delay quantity to generate may not vary, but. Like the power converter used for satellite communication, when an intermediate frequency is high, an analog filter must be used. As for the intermediate frequency of the power converter for satellite communication, near 1 GHz is mainly used.
[0007]Therefore, this invention is made in light of the above-mentioned circumstances, and the purpose, The desired characteristic is easily filled by absorbing dispersion by changing the frequency from an office, without changing the characteristic of a group-delay equalizer to change of group delay quantity, and it is in providing a cheap and small power converter.
[0008]
[Means for Solving the Problem]In order to attain said purpose, a power converter of this invention does not change the characteristic of a group delay equalizer, in order to absorb dispersion in group-delay distortion, but changes an intermediate frequency.
[0009]In a power converter which contains more an equalizer for this invention to equalize group-delay distortion generated with a band pass filter mounted in an intermediate frequency of a double conversion system in details, The 1st mixer that carries out frequency conversion of the input signal, and a synthesizer connected to a terminal from an office of said 1st mixer, It has a band pass filter connected to an output terminal of said 1st mixer, the 2nd mixer connected to an output terminal of said band pass filter, and the 2nd synthesizer connected to a terminal from an office of said 2nd mixer, and an output terminal of said 2nd mixer is considered as an output.

[0010]
[Embodiment of the Invention]An embodiment of the invention is described with reference to Drawings below. this invention -- the frequency from an office of two pieces of the composition of double conversion -- respectively -- simultaneous -- slightly high frequency -- or it changes into slightly low frequency.
[0011]Drawing 1 is a figure showing the composition of an embodiment of the invention. The 1st mixer 4 that will carry out frequency conversion of the input signal 1 if drawing 1 is referred to, The 1st synthesizer 7 connected to the terminal from an office of the 1st mixer 4, and the band pass filter 5 connected to the output terminal of the 1st mixer 4, It has the 2nd mixer 6 connected to the output terminal of the band pass filter 5, and the 2nd synthesizer 8 connected to the terminal from an office of the 2nd mixer 6, and the output of the 2nd mixer 6 is connected to the output terminal 2, and it is constituted. In drawing 1, 3 is logic for frequency setting, such as CPU, and, as for a large step synthesizer and the 2nd Shenzhen sizer 8, a small step synthesizer and 9 control [a group delay equalizer and the 1st Shenzhen sizer 7] the frequency of the 1st and 2nd Shenzhen sizer 7 and 8. Unlike the good transformation group-delay equalizer 10 of drawing 5, let the group delay equalizer 3 be a cover half.
[0012]Drawing 2 shows one working example of the fixed time delay equalizer 3. With reference to drawing 2, the equalizer input terminal 21 is connected at the node of the end of the coil 23, and the end of the capacitor 24, It is connected with one end of the capacitor 25, the other end of the coil 23 is connected to the equalizer output terminal 22, and the node of the other end of the capacitor 24 and the other end of the capacitor 25 is grounded via the capacitor 26 and the coil 27 by which the series connection was carried out.
[0013]Drawing 3 shows one working example of the synthesizer 7 of a small step. The clock from the crystal oscillator 39 is inputted into the 38 or 1/of $1/M_1$ counting-down circuit M_2 counting-down circuit 43 with reference to drawing 3, It is inputted into the frequency phase comparator (PD) 37 by the output of the counting-down circuit 38, and the frequency phase comparator 37, The frequency phase comparison result of the output of a signal and the counting-down circuit 38 which carried out dividing of the output of the mixer 34 which considers the output of the voltage controlled oscillator 33 as an input with the $1/N_1$ counting-down circuit 36 is supplied as control voltage of the voltage controlled oscillator 33 via the low pass filter (loop filter) 35. On the other hand, it is inputted into the frequency phase comparator 42 by the output of the counting-down circuit 43, and the frequency phase comparator 42, The frequency phase comparison result of the output of a signal and the counting-down circuit 43 which carried out dividing of the output of the voltage controlled oscillator 40 with the $1/N_2$ counting-down circuit 41 is supplied as control voltage of the voltage controlled oscillator 40 via the low pass filter (loop filter) 44, The output of the voltage controlled oscillator 44 is inputted into the terminal from an office of the mixer 34. The data signal from CPU9 of drawing 1 is inputted into the data input terminal 31, and the division ratio of the counting-down circuits 38, 36, 43, and 41 is set to it.
[0014]Drawing 4 shows one working example of the synthesizer 8 of a large step. With reference to drawing 4, the clock from the crystal oscillator 58 is inputted into the 1/M counting-down circuit 57, it is inputted into the frequency phase comparator 56 by counting-down circuit 57 output, and the frequency phase comparator 56, The frequency phase comparison result of the output of a signal and the counting-down circuit 57 which carried out dividing of the output of the voltage controlled oscillator 53 with the counting-down circuit 55 is supplied as control voltage of the voltage controlled oscillator 53 via the low pass filter 54, and the oscillation output

of the voltage controlled oscillator 53 is supplied to the terminal from an office of the 2nd mixer 6. The data signal from CPU9 of drawing 1 is inputted into the terminal 51, and the division ratio of the counting-down circuits 57 and 55 is set up.
[0015]For the miniaturization of a power converter, and low-cost-izing, easy digitization of adjustment is indispensable.
[0016]It is difficult in cost for the band pass filter which dispersion generates to lose ********** in analog circuitry.
[0017]Since the good transformation group-delay equalizer 10 in the conventional frequency changing circuit shown in drawing 5 is also analog circuitry on the other hand, Since an analog/digital one, and a digital to analog are needed for digitizing, when composition becomes large and group delay quantity is changed with a good transformation group-delay equalizer, the difficulty of adjustment -- there is the necessity of returning change of an amplitude frequency characteristic -- is also produced.
[0018]By the way, the group-delay distortion of a power converter is produced with the band pass filter (5 of drawing 1) mounted in the intermediate frequency.
[0019]As an example, the synthesizer of 1 GHz and the 2nd from game in the 1st from game of 70 MHz/6GHz transmit frequency inverter used by the transmission system of satellite communication is 5 GHz on the problem of a spurious signal in many cases.
[0020]The intermediate frequency in this case is near 1 GHz, and in order to realize small, the band pass filter comprises a dielectric element.
[0021]If dispersion in this band pass filter is lost, dispersion in the group delay frequency characteristics of a power converter will not be produced, either, but manufacturing dispersion cannot be stopped actually. Since manufacturing dispersion is stopped, cost cannot be lowered when strict adjustment or sorting is performed.
[0022]However, as for it, dispersion in the group delay frequency characteristics of a band pass filter turns out that the most is dispersion in center frequency.
[0023]For example, when dispersion in the center frequency of a 1-GHz band pass filter is about 0.2%, a gap of the center frequency of group-delay distortion which has secondary curvature is set to 2 MHz. Since a center gap of 2-MHz group-delay distortion was equalized, as described above, with the conventional composition, it was absorbing with the good transformation group-delay equalizer 10 (refer to drawing 5).
[0024]However, in an embodiment of the invention, temporarily, when there are 2 MHz of center gaps of group-delay distortion, the 1st from game and the 2nd 2 MHz from game are shifted.
[0025]When the 2nd from game is 4900 MHz as an example, in order for the 1st from game to absorb dispersion in group-delay distortion at 1030 MHz at the beginning, the 1st from game is changed into 1032 MHz, and the 2nd from game is changed into 4902 MHz.
[0026]That is, even if it sets it as the same output frequency, the 1st [in all] from game, the 2nd from game, and an intermediate frequency are changed into a gap of the band pass filter 5.
[0027]And at the time of production, the frequency of a gap of a band pass filter performs initial setting so that group-delay distortion may become small most.
[0028]In an embodiment of the invention, although the 1st from game needs to change into a synthesizer the portion which was a fixed local conventionally, Composition does not become complicated, in order to comprise a digital PLL circuit from the first and to only change the division ratio (counting-down circuits 57 and 55), as shown in drawing 4.
[0029]Since the frequency revision from the 1st game is only for absorbing dispersion in group

delay quantity, it does not require the small step which makes a 575-MHz zone lock at 125 kHz like the synthesizer 7 from the 2nd game.
[0030]For this reason, there is an at most 1-MHz step, and sufficient zone to be changed is about **5 MHz.
[0031]For this reason, since the 2nd synthesizer 8 can be constituted from a digital PLL circuit of single looping as shown in drawing 4, the difference from the conventional system shown in drawing 5 currently used on the fixed local serves as [whether the data for initial setting is only received from the exterior, and] a chisel.
[0032]Since dispersion is absorbed by changing the frequency from an office in this way according to the embodiment of the invention, without changing the characteristic of a group-delay equalizer to change of group delay quantity, the characteristic can be satisfied easily.
[0033]
[Effect of the Invention]As explained above, according to this invention, since it is not necessary to use a variable group-delay equalizer like before, the effect that a cheap and small power converter is realizable is done so.

TECHNICAL FIELD

[Field of the Invention]Especially this invention relates to the power converter formed in the transmission system or receiving system of a satellite communication device about a power converter.

PRIOR ART

[Description of the Prior Art]Conventionally, in this kind of power converter, in order that the group-delay equalizer for equalizing group-delay distortion may absorb manufacturing dispersion, the variable function is needed.
[0003]Although the composition of the large good transformation time delay equalizer of the variable range of the amount of group delay equalization is proposed by JP,H03-040534,B as a variable group-delay equalizer, without having an adverse effect on an amplitude frequency characteristic, After changing group delay quantity since the amplitude frequency characteristic of the group-delay equalizer itself is changed when changing group delay quantity, it is necessary to return degradation of an amplitude frequency characteristic.
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EFFECT OF THE INVENTION

[Effect of the Invention]As explained above, according to this invention, since it is not necessary to use a variable group-delay equalizer like before, the effect that a cheap and small power converter is realizable is done so.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention]However, in order to realize a cheap and small power converter, it is necessary to absorb dispersion easily. Or what is necessary is just to make it not generate dispersion in group delay quantity.
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MEANS

[Means for Solving the Problem]In order to attain said purpose, a power converter of this invention does not change the characteristic of a group delay equalizer, in order to absorb dispersion in group-delay distortion, but changes an intermediate frequency.
[0009]In a power converter which contains more an equalizer for this invention to equalize group-delay distortion generated with a band pass filter mounted in an intermediate frequency of a double conversion system in details, The 1st mixer that carries out frequency conversion of the input signal, and a synthesizer connected to a terminal from an office of said 1st mixer, It has a band pass filter connected to an output terminal of said 1st mixer, the 2nd mixer connected to an output terminal of said band pass filter, and the 2nd synthesizer connected to a terminal from an office of said 2nd mixer, and an output terminal of said 2nd mixer is considered as an output.
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[0018]By the way, the group-delay distortion of a power converter is produced with the band

pass filter (5 of drawing 1) mounted in the intermediate frequency.
[0019]As an example, the synthesizer of 1 GHz and the 2nd from game in the 1st from game of 70 MHz/6GHz transmit frequency inverter used by the transmission system of satellite communication is 5 GHz on the problem of a spurious signal in many cases.
[0020]The intermediate frequency in this case is near 1 GHz, and in order to realize small, the band pass filter comprises a dielectric element.
[0021]If dispersion in this band pass filter is lost, dispersion in the group delay frequency characteristics of a power converter will not be produced, either, but manufacturing dispersion cannot be stopped actually. Since manufacturing dispersion is stopped, cost cannot be lowered when strict adjustment or sorting is performed.
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[0023]For example, when dispersion in the center frequency of a 1-GHz band pass filter is about 0.2%, a gap of the center frequency of group-delay distortion which has secondary curvature is set to 2 MHz. Since a center gap of 2-MHz group-delay distortion was equalized, as described above, with the conventional composition, it was absorbing with the good transformation group-delay equalizer 10 (refer to drawing 5).
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[0032]Since dispersion is absorbed by changing the frequency from an office in this way according to the embodiment of the invention, without changing the characteristic of a group-delay equalizer to change of group delay quantity, the characteristic can be satisfied easily.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1]It is a figure showing the composition of an embodiment of the invention.
[Drawing 2]It is a figure showing one working example of the group delay equalizer of the immobilization in an embodiment of the invention.
[Drawing 3]It is a figure showing one working example of the small step synthesizer in an embodiment of the invention.
[Drawing 4]It is a figure showing one working example of the large step synthesizer in an embodiment of the invention.
[Drawing 5]It is a figure showing the composition of the conventional power converter.
[Description of Notations]
1 Input terminal
2 Output terminal
3 Group delay equalizer
4 and 6 Mixer
5 Band pass filter
7 Large step synthesizer
8 Small step synthesizer
9 Logic for frequency setting
10 Good transformation group-delay equalizer
11 Phase lock oscillator
21 Equalizer input terminal
22 Equalizer output terminal
23 and 27 Coil
24, 25, and 26 Capacitor
31 Synthesizer input terminal
32 Synthesizer output terminal
33 and 40 Voltage controlled oscillator
34 Mixer
35 and 44 Low pass filter
36, 38, 41, and 43 Counting-down circuit
37 and 42 Frequency phase comparator
39 Crystal oscillator
51 Synthesizer input terminal
52 Synthesizer output terminal
53 Voltage controlled oscillator
54 Low pass filter
35 and 57 Counting-down circuit
56 Frequency phase comparator
58 Crystal oscillator

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報（Ａ）**　(11)特許出願公開番号

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(43)公開日　平成10年(1998)５月29日

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Ｈ０３Ｄ　7/16		Ｈ０３Ｄ　7/16		

審査請求　有　　請求項の数４　ＦＤ　（全　６　頁）

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(22)出願日　平成８年(1996)11月８日

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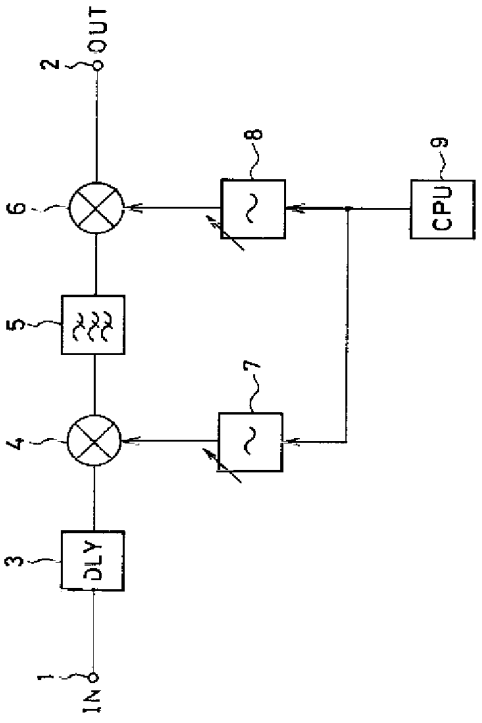
(54)【発明の名称】　周波数変換装置

(57)【要約】
【課題】群遅延量の変動に対して群遅延等化器の特性を変更することなく、局発の周波数を変更することによってばらつきを吸収することにより、所望の特性を容易に満たすと共に、安価且つ小型の周波数変換装置の提供。
【解決手段】ダブルコンバージョン方式の中間周波数に実装されたバンドパスフィルタで発生する群遅延歪を等化するための等化器を内蔵する周波数変換装置において、入力信号を周波数変換する第１の混合器４と、第１の混合器の局発端子に接続された第１のシンセサイザ７と、第１の混合器の出力端子に接続されたバンドパスフィルタ５と、バンドパスフィルタの出力端子に接続された第２の混合器６と、第２の混合器の局発端子に接続された第２のシンセサイザ８と、を備え、第２の混合器の出力端子を出力とする。



【特許請求の範囲】
【請求項１】ダブルコンバージョン方式の中間周波数に実装されたバンドパスフィルタで発生する群遅延歪を等化するための等化器を内蔵する周波数変換装置において、
入力信号を周波数変換する第１の混合器と、
前記第１の混合器の局発端子に接続された第１のシンセサイザと、
前記第１の混合器の出力端子に接続されたバンドパスフィルタと、
前記バンドパスフィルタの出力端子に接続された第２の混合器と、
前記第２の混合器の局発端子に接続された第２のシンセサイザと、
を備え、
前記第２の混合器の出力端子を出力とする、
ことを特徴とする周波数変換装置。
【請求項２】群遅延等化器、第１の混合器、バンドパスフィルタ、及び第２の混合器を備えてなる周波数変換装置において、
前記バンドパスフィルタにおける群遅延量の変動に対応させて、前記第１、及び第２の混合器の局発端子の周波数を変更することによって、前記群遅延等化器の特性を可変とせずに、群遅延歪のばらつきを吸収するようにした、ことを特徴とする周波数変換装置。
【請求項３】ダブルコンバージョン方式の中間周波数に実装されたバンドパスフィルタで発生する群遅延歪を等化するための等化器を内蔵する周波数変換装置において、
入力信号を周波数変換する第１の混合器と、
前記第１の混合器の局発端子に接続された第１のシンセサイザと、
前記第１の混合器の出力端子に接続されたバンドパスフィルタと、
前記バンドパスフィルタの出力端子に接続された第２の混合器と、
前記第２の混合器の局発端子に接続された第２のシンセサイザと、
を備え、
前記第２の混合器の出力端子を出力とし、
前記バンドパスフィルタの群遅延歪のセンターずれに合わせて前記第１、第２のシンセサイザの出力周波数を可変させ、これにより群遅延歪のばらつきを吸収する、
ことを特徴とする周波数変換装置。
【請求項４】前記第１及び第２のシンセサイザがディジタルＰＬＬ回路で構成され、前記第２のシンセサイザが前記第１のシンセサイザよりも周波数ステップが粗く設定可とされたことを特徴とする請求項３記載の周波数変換装置。
【発明の詳細な説明】
【０００１】
【発明の属する技術分野】本発明は、周波数変換装置に関し、特に衛星通信装置の送信系または受信系に設けられる周波数変換装置に関する。
【０００２】
【従来の技術】従来、この種の周波数変換装置において、群遅延歪を等化するための群遅延等化器は、製造上のばらつきを吸収するために可変機能が必要とされている。
【０００３】可変の群遅延等化器として、特公平０３－０４０５３４号公報には、振幅周波数特性に悪影響を与えることなく群遅延時間等化量の可変範囲の広い可変型遅延時間等化器の構成が提案されているが、群遅延量を変更するときに、群遅延等化器自体の振幅周波数特性が変動するため群遅延量を変更した後に、振幅周波数特性の劣化を戻す必要がある。
【０００４】図５は、従来の周波数変換装置の構成を示す図である。図５を参照すると、従来の周波数変換装置は、入力信号を周波数変換する第１の混合器４と、第１の混合器４の局発端子に接続された位相同期発振器１１と、第１の混合器４の出力端子に接続されたバンドパスフィルタ５と、バンドパスフィルタ５の出力端子に接続された第２の混合器６と、第２の混合器６の局発端子に接続されたシンセサイザ８と、を備え、第２の混合器６の出力を出力端子２に接続して構成されている。９はＣＰＵ等の周波数設定用ロジック、１０は可変型群遅延等化器である。群遅延歪のずれを等化するために、従来の構成では、可変型群遅延等化器１０で吸収していた。
【０００５】
【発明が解決しようとする課題】しかしながら、安価かつ小型の周波数変換装置を実現するためには、容易にばらつきを吸収する必要がある。あるいは、群遅延量のばらつきを発生しないようにすれば良い。
【０００６】この場合、中間周波数が低い場合には、例えば特開昭６０－１１７９２６号公報に提案されるように、発生する群遅延量がばらつかないようにディジタルフィルタを使用することで群遅延量のばらつきの問題を解決することもできるが、衛星通信に使用する周波数変換装置のように、中間周波数が高い場合には、アナログフィルタを使用せざるを得ない。衛星通信用周波数変換装置の中間周波数は、おもに１ＧＨｚ付近が使用される。
【０００７】したがって、本発明は、上記事情に鑑みてなされたものであって、その目的は、群遅延量の変動に対して群遅延等化器の特性を変更することなく、局発の周波数を変更することによってばらつきを吸収することにより、所望の特性を容易に満たすと共に、安価且つ小型の周波数変換装置を提供することにある。
【０００８】
【課題を解決するための手段】前記目的を達成するた

め、本発明の周波数変換装置は、群遅延歪のばらつきを吸収するために群遅延時間等化器の特性を変更するのでなく、中間周波数を変更するようにしたものである。

【０００９】より詳細には、本発明は、ダブルコンバージョン方式の中間周波数に実装されたバンドパスフィルタで発生する群遅延歪を等化するための等化器を内蔵する周波数変換装置において、入力信号を周波数変換する第１の混合器と、前記第１の混合器の局発端子に接続されたシンセサイザと、前記第１の混合器の出力端子に接続されたバンドパスフィルタと、前記バンドパスフィルタの出力端子に接続された第２の混合器と、前記第２の混合器の局発端子に接続された第２のシンセサイザと、を備え、前記第２の混合器の出力端子を出力とする、ことを特徴とする。

【００１０】

【発明の実施の形態】本発明の実施の形態について以下に図面を参照して説明する。本発明は、ダブルコンバージョンの構成の２個の局発周波数をそれぞれ同時にわずかに高い周波数かまたはわずかに低い周波数に変更するものである。

【００１１】図１は、本発明の実施の形態の構成を示す図である。図１を参照すると、入力信号１を周波数変換する第１の混合器４と、第１の混合器４の局発端子に接続された第１のシンセサイザ７と、第１の混合器４の出力端子に接続されたバンドパスフィルタ５と、バンドパスフィルタ５の出力端子に接続された第２の混合器６と、第２の混合器６の局発端子に接続された第２のシンセサイザ８と、を備え、第２の混合器６の出力を出力端子２に接続して構成されている。図１において、３は群遅延時間等化器、第１のシンセンサイザ７はラージステップシンセサイザ、第２のシンセンサイザ８はスモールステップシンセサイザ、また９はＣＰＵ等の周波数設定用ロジックであり、第１、第２のシンセンサイザ７、８の周波数を制御する。群遅延時間等化器３は、図５の可変型群遅延等化器１０と異なり、固定型とされる。

【００１２】図２は、固定の遅延時間等化器３の一実施例を示している。図２を参照して、等化器入力端子２１は、コイル２３の一端とコンデンサ２４の一端の接続点に接続され、コイル２３の他端はコンデンサ２５の一端と接続されて等化器出力端子２２に接続され、コンデンサ２４の他端とコンデンサ２５の他端の接続点は、直列接続されたコンデンサ２６とコイル２７を介して接地されている。

【００１３】図３は、スモールステップのシンセサイザ７の一実施例を示している。図３を参照して、クリスタル発振器３９からのクロックは１／M_1分周器３８、１／M_2分周器４３に入力されており、分周器３８の出力は周波数位相比較器（ＰＤ）３７に入力され、周波数位相比較器３７は、電圧制御発振器３３の出力を入力とする混合器３４の出力を１／N_1分周器３６で分周した信号と分周器３８の出力の周波数位相比較結果をローパスフィルタ（ループフィルタ）３５を介して電圧制御発振器３３の制御電圧として供給する。一方、分周器４３の出力は周波数位相比較器４２に入力され、周波数位相比較器４２は、電圧制御発振器４０の出力を１／N_2分周器４１で分周した信号と分周器４３の出力の周波数位相比較結果をローパスフィルタ（ループフィルタ）４４を介して電圧制御発振器４０の制御電圧として供給し、電圧制御発振器４４の出力は混合器３４の局発端子に入力されている。また、データ入力端子３１には、図１のＣＰＵ９からのデータ信号が入力され、分周器３８、３６、４３、及び４１の分周比を設定する。

【００１４】図４は、ラージステップのシンセサイザ８の一実施例を示している。図４を参照して、クリスタル発振器５８からのクロックは１／Ｍ分周器５７に入力され、分周器５７出力は周波数位相比較器５６に入力され、周波数位相比較器５６は、電圧制御発振器５３の出力を分周器５５で分周した信号と分周器５７の出力の周波数位相比較結果をローパスフィルタ５４を介して電圧制御発振器５３の制御電圧として供給し、電圧制御発振器５３の発振出力が第２の混合器６の局発端子に供給される。端子５１には図１のＣＰＵ９からのデータ信号が入力され、分周器５７、５５の分周比を設定する。

【００１５】周波数変換装置の小型化と低コスト化のためには調整の容易なディジタル化が欠かせない。

【００１６】ばらつきが発生するバンドパスフィルタがアナログ回路でりばらつきをなくすことはコスト的に困難である。

【００１７】一方、図５に示した従来の周波数変換回路における可変型群遅延等化器１０もアナログ回路であるため、ディジタル化するにはアナログ／ディジタル、ディジタル／アナログ変換が必要とされるため、構成が大きくなり、また可変型群遅延等化器で群遅延量を変更する際には、振幅周波数特性の変動を戻す必要があるなど調整の困難さも生じる。

【００１８】ところで、周波数変換装置の群遅延歪は、中間周波数に実装されたバンドパスフィルタ（図１の５）で生じる。

【００１９】一例として、衛星通信の送信系で使用する７０ＭＨｚ／６ＧＨｚ送信周波数変換装置は、スプリアス信号の問題で、第１局発が１ＧＨｚ、第２局発のシンセサイザが５ＧＨｚであることが多い。

【００２０】この場合の中間周波数は１ＧＨｚ付近であり、小型に実現するために、バンドパスフィルタは誘電体素子で構成されている。

【００２１】このバンドパスフィルタのばらつきを無くせば周波数変換装置の群遅延特性のばらつきも生じないが、実際には製造上のばらつきを抑えることはできない。製造上のばらつきを抑えるため、厳密な調整または選別を行なった場合コストを下げることはできない。

【００２２】しかし、バンドパスフィルタの群遅延特性のばらつきは、そのほとんどが中心周波数のばらつきであることが分かっている。

【００２３】例えば、１ＧＨｚバンドパスフィルタの中心周波数のばらつきが約０．２％であった場合、２次曲率を有する群遅延歪の中心周波数のずれは２ＭＨｚとなる。２ＭＨｚの群遅延歪のセンターずれを等化するために、従来の構成では、上記したように、可変型群遅延等化器１０（図５参照）で吸収していた。

【００２４】しかし、本発明の実施の形態においては、仮に、群遅延歪のセンターずれが２ＭＨｚある場合には、第１局発と第２局発を２ＭＨｚずらす。

【００２５】一例として、当初第１局発が１０３０ＭＨｚで、第２局発が４９００ＭＨｚであったとき、群遅延歪のばらつきを吸収するために、第１局発を１０３２ＭＨｚ、第２局発を４９０２ＭＨｚに変更する。

【００２６】すなわち同じ出力周波数に設定しても、バンドパスフィルタ５のずれに合わせて第１局発と第２局発、中間周波数を変える。

【００２７】そして、バンドパスフィルタのずれの周波数は、生産時に、最も群遅延歪が小さくなるよう初期設定を行なう。

【００２８】本発明の実施の形態において、第１局発は、従来固定ローカルであった部分をシンセサイザに変更する必要があるが、図４に示すように、もともとディジタルＰＬＬ回路で構成されており、その分周比（分周器５７、５５）を変更するだけであるため、構成が複雑になることはない。

【００２９】第１局発の周波数変更は、群遅延量のばらつきを吸収するためだけであるため、第２局発のシンセサイザ７のように５７５ＭＨｚの帯域を１２５ＫＨｚでロックさせるスモールステップを要求するものでない。

【００３０】このため、たかだか１ＭＨｚステップもあれば十分であり、かつ変更が必要な帯域も±５ＭＨｚ程度である。

【００３１】このため、第２のシンセサイザ８は、図４に示すように、シングルループ型のディジタルＰＬＬ回路で構成することができるため、固定ローカルで使用している図５に示した従来方式との違いは、単に外部から初期設定用データを受けるかどうかのみとなる。

【００３２】本発明の実施の形態によれば、このように、群遅延量の変動に対して群遅延等化器の特性を変更することなく、局発の周波数を変更することによってばらつきを吸収しているため、容易に特性を満足することができる。

【００３３】

【発明の効果】以上説明したように、本発明によれば、従来のように可変の群遅延等化器を使用する必要がないため、安価にかつ小型の周波数変換装置を実現することができるという効果を奏する。

【図面の簡単な説明】

【図１】本発明の実施の形態の構成を示す図である。

【図２】本発明の実施の形態における固定の群遅延時間等化器の一実施例を示す図である。

【図３】本発明の実施の形態におけるスモールステップシンセサイザの一実施例を示す図である。

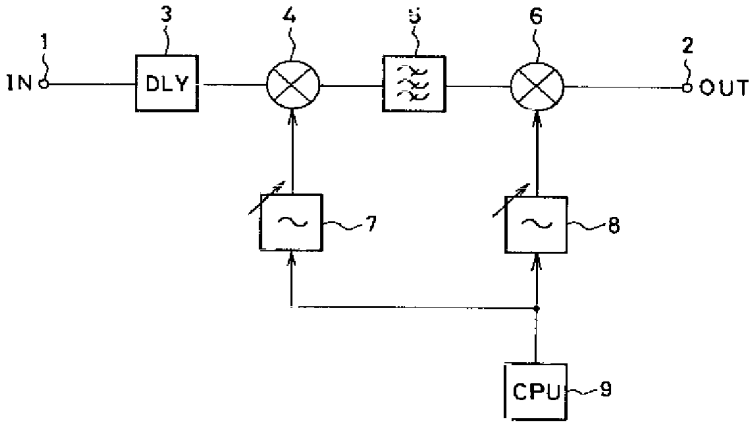
【図４】本発明の実施の形態におけるラージステップシンセサイザの一実施例を示す図である。

【図５】従来の周波数変換装置の構成を示す図である。

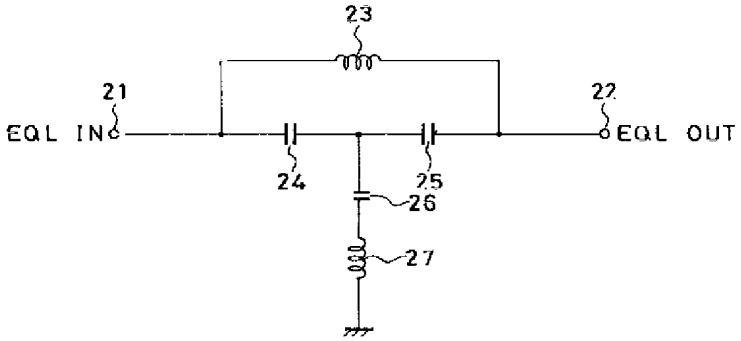
【符号の説明】

１　入力端子
２　出力端子
３　群遅延時間等化器
４、６　混合器
５　バンドパスフィルタ
７　ラージステップシンセサイザ
８　スモールステップシンセサイザ
９　周波数設定用ロジック
１０　可変型群遅延等化器
１１　位相同期発振器
２１　等化器入力端子
２２　等化器出力端子
２３、２７　コイル
２４、２５、２６　コンデンサ
３１　シンセサイザ入力端子
３２　シンセサイザ出力端子
３３、４０　電圧制御発振器
３４　混合器
３５、４４　ローパスフィルタ
３６、３８、４１、４３　分周器
３７、４２　周波数位相比較器
３９　クリスタル発振器
５１　シンセサイザ入力端子
５２　シンセサイザ出力端子
５３　電圧制御発振器
５４　ローパスフィルタ
３５、５７　分周器
５６　周波数位相比較器
５８　クリスタル発振器

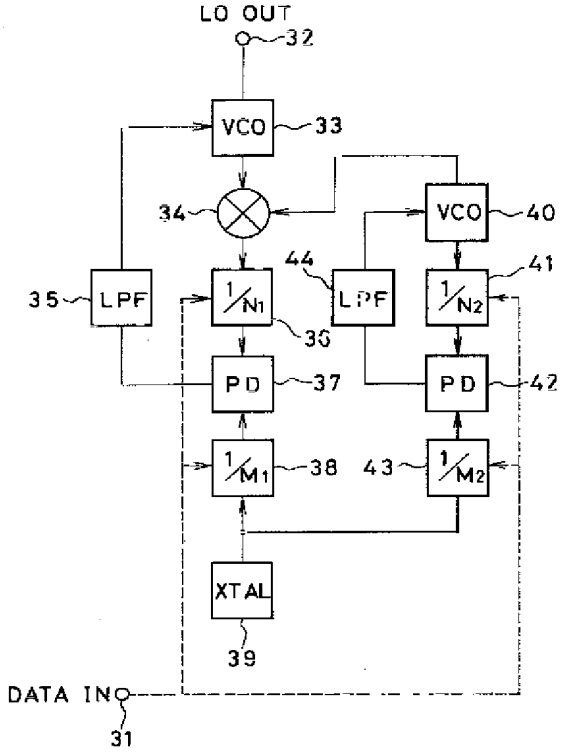
【図１】


1
IN
3
DLY
4
5
6
2
OUT
7
8
CPU
9

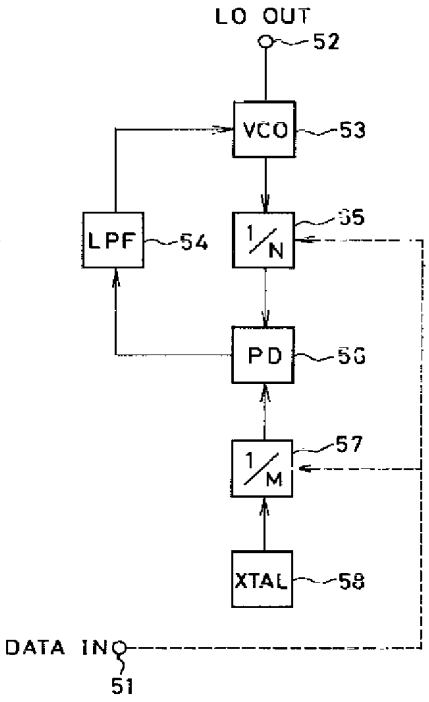
【図２】


23
21
EQL IN
22
EQL OUT
24
25
26
27

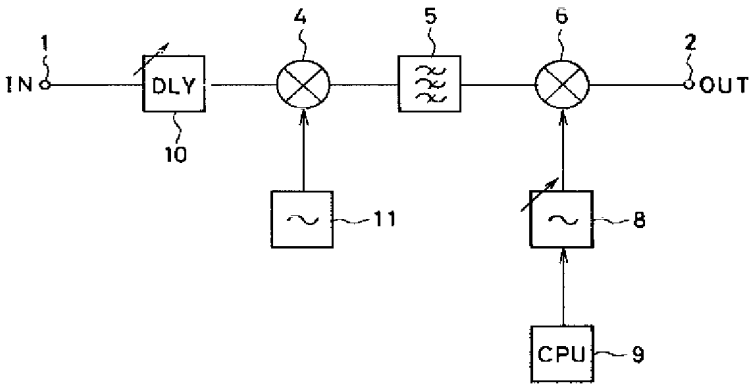
【図３】


LO OUT
32
VCO
33
34
VCO
40
44
41
35
LPF
1/N1
LPF
1/N2
36
PD
37
PD
42
1/M1
38
43
1/M2
XTAL
39
DATA IN
31

【図４】


LO OUT
52
VCO
53
LPF
54
1/N
55
PD
56
1/M
57
XTAL
58
DATA IN
51

【図５】


1
IN
DLY
10
4
11
5
6
8
2
OUT
CPU
9